5 V Single Supply, 8-Channel, 14-Bit 285 kSPS Sampling ADC

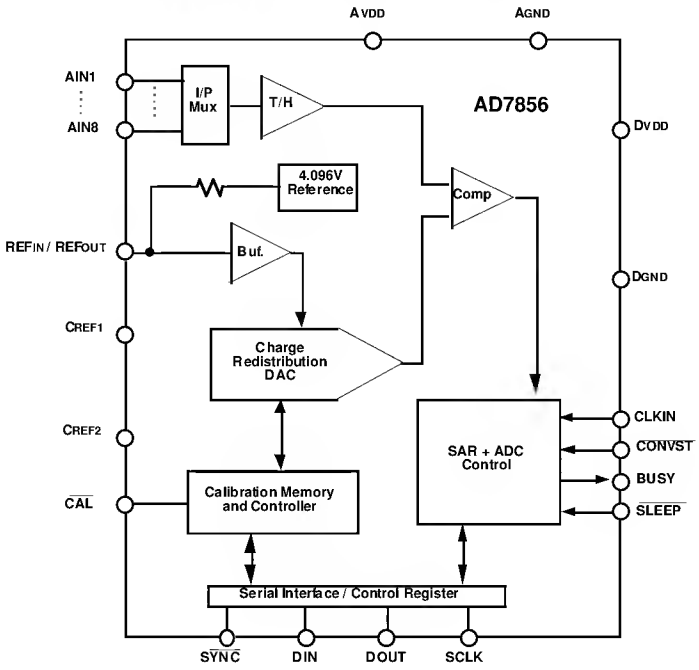
Preliminary Technical Data

AD7856*

FEATURES
Single 5 V Supply
285 kSPS Throughput Rate
System and Self-Calibration with Autocalibration on Power-Up
Eight Single-Ended or Four Pseudo-Differential Inputs
Low Power: 60 mW typ
Automatic Power Down After Conversion (5 uW)
Flexible Serial Interface:
8051/SPI/QSPI/mP Compatible
24-Pin DIP, SOIC and SSOP Packages

APPLICATIONS
Battery-Powered Systems (Personal Digital Assistants, Medical Instruments, Mobile Communications)
Pen Computers
Instrumentation and Control Systems
High Speed Modems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7856 are high speed, low power, 14-bit ADCs that operate from a single 5 V power supply. The ADC powers up with a set of default conditions at which time it can be operated as a read only ADC. The ADC contains self-calibration and system calibration options to ensure accurate operation over time and temperature and have a number of power-down options for low power applications. The part powers up with a set of default conditions and can operate as a read only ADC.

The AD7856 is capable of 285 kHz throughput rate. The input track-and-hold acquires a signal in 500 ns and features a pseudo-differential sampling scheme. The AD7856 voltage range is 0 to V_{REF} with both straight binary and 2s complement output coding. Input signal range is to the supply and the part is capable of converting full power signals to 100 kHz.

CMOS construction ensures low power dissipation of typically 5.4 mW for normal operation and 3.6 μW in power-down mode. The part is available in 24-pin, 0.3 inch-wide dual-in-line package (DIP), 24-lead small outline (SOIC) and 24-lead small shrink outline (SSOP) packages.

PRODUCT HIGHLIGHTS

1. Single 5 V supply.
2. Automatic calibration on power-up.
3. Flexible power management options including automatic powerdown after conversion.
4. Operates with reference voltages from 1.2 V to V_{DD}.
5. Analog input range from 0 V to V_{DD}.
6. Eight single-ended or four pseudo-differential input channels.
7. Self- and system calibration.
8. Versatile serial I/O port (SPI/QSPI/8051/μP).

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AD7856– SPECIFICATIONS[1, 2]

A Grade: f_{CLKIN} = 6 MHz, (– 40°C to +85°C), f_{SAMPLE} = 285 kHz; K Grade: f_{CLKIN} = 6 MHz, (0°C to +85°C), f_{SAMPLE} = 285 kHz;(AV_{DD} = DV_{DD} = +5.0 V ±5% ., REF_{IN}/REF_{OUT} = 4.096 V External Reference unless otherwise noted, $\overline{SLEEP}$ = Logic High; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]	K Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE				
Signal to Noise + Distortion Ratio[3] (SNR)	78	78	dB min	Typically SNR is 79.5 dB V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 285 kHz
Total Harmonic Distortion (THD)	–86	–86	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 285 kHz
Peak Harmonic or Spurious Noise	–87	–87	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 285 kHz
Intermodulation Distortion (IMD)				
Second Order Terms	–86	–90	dB typ	fa = 9.983 kHz, fb = 10.05 kHz, f_{SAMPLE} = 285 kHz
Third Order Terms	–86	–90	dB typ	fa = 9.983 kHz, fb = 10.05 kHz, f_{SAMPLE} = 285 kHz
Channel-to-Channel Isolation	–90	–90	dB typ	V_{IN} = 25 kHz
DC ACCURACY				Any Channel
Resolution	14	14	Bits	
Integral Nonlinearity	±2	±1	LSB max	4.096 V External Reference, V_{DD} = 5 V
Differential Nonlinearity	±2	±1	LSB max	Guaranteed No Missed Codes to 14 Bits.
Total Unadjusted Error	±1	±1	LSB typ	
Unipolar Offset Error	±10	±10	LSB max	Typically ±2 LSBs
Unipolar Offset Error Match			LSB max	
Positive Full-Scale Error	±10	±10	LSB max	
Positive Full-Scale Error Match			LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{REF}	0 to V_{REF}	Volts	i.e., AIN(+) – AIN(–) = 0 to V_{REF}, AIN(–) can be biased up but AIN(+) cannot go below AIN(–)
Leakage Current	±1	±1	µA max	
Input Capacitance	20	20	pF typ	
REFERENCE INPUT/OUTPUT				
REF_{IN} Input Voltage Range	$4.096/V_{DD}$	$2.3/V_{DD}$	V min/max	Functional from 1.2 V
Input Impedance	150	150	kΩ typ	Resistor connected to Internal Reference Node
REF_{OUT} Output Voltage	3.696/4.496	3.696/4.496	V min/max	
REF_{OUT} Tempco	20	20	ppm/°C typ	
LOGIC INPUTS				
Input High Voltage, V_{INH}	V_{DD} - 1.0	V_{DD} - 1.0	V min	
Input Low Voltage, V_{INL}	0.4	0.4	V max	
Input Current, I_{IN}	±10	±10	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[4]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{DD} - 0.4	V_{DD} - 0.4	V min	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6 mA
Floating-State Leakage Current	±10	±10	µA max	
Floating-State Output Capacitance[4]	10	10	pF max	
Output Coding	Straight (Natural) Binary			Unipolar Input Range
CONVERSION RATE				
Conversion Time	3.33	3.33	µs max	21 CLKIN cycles
Track/Hold Acquisition Time	0.33	0.33	µs min	

Parameter	A Version[1]	K Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE				
AV_{DD}, DV_{DD}	+4.75/+5.25	+4.75/+5.25	V min/max	
I_{DD}				
Normal Mode[5]	17	17	mA max	$AV_{DD} = DV_{DD}$ = 4.5 V to 5.5 V. Typically 12 mA
Sleep Mode[6]				
With External Clock On	10	10	μA typ	Full Power Down. Power Management Bits in Control Register Set as PMGT1 = 1, PMGT0 = 0
	400	400	μA typ	Partial Power Down. Power Management Bits in Control Register Set as PMGT1 = 1, PMGT0 = 1
With External Clock Off	5	5	μA max	Typically 1 μA. Full Power Down. Power Management Bits in Control Register Set as PMGT1 = 1, PMGT0 = 0
	200	200	μA typ	Partial Power Down. Power Management Bits in Control Register Set as PMGT1 = 1, PMGT0 = 1
Normal Mode Power Dissipation	78.75	78.75	mW max	V_{DD} = 5.25 V. Typically 60 mW; $\overline{SLEEP} = V_{DD}$
Sleep Mode Power Dissipation				
With External Clock On	52.5	52.5	μW typ	V_{DD} = 5.25 V. $\overline{SLEEP}$ = 0 V
With External Clock Off	26.25	26.25	μW max	V_{DD} = 5.25 V. Typically 5.25 μW; $\overline{SLEEP}$ = 0 V
SYSTEM CALIBRATION				
Offset Calibration Span[7]	$+0.05 \times V_{REF}/-0.05 \times V_{REF}$		V max/min	Allowable Offset Voltage Span for Calibration
Gain Calibration Span[7]	$+1.025 \times V_{REF}/-0.975 \times V_{REF}$		V max/min	Allowable Full-Scale Voltage Span for Calibration

NOTES

[1]Temperature ranges as follows: A Version: –40°C to +85°C. K Version: 0°C to +70°C

[2]Specifications apply after calibration.

[3]SNR calculation includes distortion and noise components.

[4]Sample tested @ +25°C to ensure compliance.

[5]All digital inputs @ DGND except for $\overline{CONVST}$, $\overline{SLEEP}$, $\overline{CAL}$, and $\overline{SYNC}$ @ DV_{DD}. No load on the digital outputs. Analog inputs @ AGND.

[6]CLKIN @ DGND when external clock off. All digital inputs @ DGND except for $\overline{CONVST}$, $\overline{SLEEP}$, $\overline{CAL}$, and $\overline{SYNC}$ @ DV_{DD}. No load on the digital outputs. Analog inputs @ AGND.

[7]The Offset and Gain Calibration Spans are defined as the range of offset and gain errors that the AD7856 can calibrate. Note also that these are voltage spans and are not absolute voltages (i.e., the allowable system offset voltage presented at AIN(+) for the system offset error to be adjusted out will be AIN(–) $\pm 0.05 \times V_{REF}$, and the allowable system full scale voltage applied between AIN(+) and AIN(–) for the system full-scale voltage error to be adjusted out will be $V_{REF} \pm 0.025 \times V_{REF}$). This is explained in more detail in the Calibration section of the data sheet.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (AV_{DD} = DV_{DD} = +5.0 V; f_{CLKIN} = 6 MHz; T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	Limit at T_{MIN}, T_{MAX} (A, K Versions) 5 V	Units	Description
f_{CLKIN}[2]	500	kHz min	Master Clock Frequency
	6	MHz max	
f_{SCLK}	10	MHz max	
t_1[3]	100	ns min	$\overline{CONVST}$ Pulse Width
t_2	50	ns max	$\overline{CONVST}$↓ to BUSY↑ Propagation Delay
$t_{CONVERT}$	3.33	μs max	Conversion Time = 20 t_{CLKIN}
t_3	–0.4 t_{SCLK}	ns min	$\overline{SYNC}$↓ to SCLK↓ Setup Time (Noncontinuous SCLK Input)
	70.4 t_{SCLK}	ns min/max	$\overline{SYNC}$↓ to SCLK↓ Setup Time (Continuous SCLK Input)
t_4[4]	30	ns max	Delay from $\overline{SYNC}$↓ Until DOUT 3-State Disabled
t_5[4]	30	ns max	Delay from $\overline{SYNC}$↓ Until DIN 3-State Disabled
t_6[4]	45	ns max	Data Access Time After SCLK↓
t_7	30	ns min	Data Setup Time Prior to SCLK↑
t_8	20	ns min	Data Valid to SCLK Hold Time
t_9	0.4 t_{SCLK}	ns min	SCLK High Pulse Width
t_{10}	0.4 t_{SCLK}	ns min	SCLK Low Pulse Width
t_{11}	30	ns min	SCLK↑ to $\overline{SYNC}$↑ Hold Time (Noncontinuous SCLK)
	30/0.4 t_{SCLK}	ns min/max	(Continuous SCLK)
t_{12}[5]	50	ns max	Delay from $\overline{SYNC}$↑ Until DOUT 3-State Enabled
t_{13}	90	ns max	Delay from SCLK↑ to DIN Being Configured as Output
t_{14}[6]	50	ns max	Delay from SCLK↑ to DIN Being Configured as Input
t_{15}	2.5 t_{CLKIN}	ns max	$\overline{CAL}$↑ to BUSY↑ Delay
t_{16}	2.5 t_{CLKIN}	ns max	$\overline{CONVST}$↓ to BUSY↑ Delay in Calibration Sequence
t_{CAL}[7]	83.3	ms typ	Full Self-Calibration Time, Master Clock Dependent (500052 t_{CLKIN})
t_{CAL1}[7]	74.1	ms typ	Internal DAC Plus System Full-Scale Cal Time, Master Clock Dependent (444456 t_{CLKIN})
t_{CAL2}[7]	9.25	ms typ	System Offset Calibration Time, Master Clock Dependent (55596 t_{CLKIN})
t_{Delay}	65	ns max	Delay from CLK to SCLK

NOTES

Descriptions that refer to SCLK↑ (rising) or SCLK↓ (falling) edges here are with the POLARITY pin HIGH. For the POLARITY pin LOW then the opposite edge of SCLK will apply.

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V. See Table XI and timing diagrams for different interface modes and Calibration.

[2]Mark/Space ratio for the master clock input is 40/60 to 60/40.

[3]The $\overline{CONVST}$ pulse width will here only applies for normal operation. When the part is in power-down mode, a different $\overline{CONVST}$ pulse width will apply (see Power-Down section).

[4]Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.4 V.

[5]t_{12} is derived form the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time, t_{12}, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

[6] t_{14} is derived form the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time quoted in the Timing Characteristics is the true delay of the part in turning off the output drivers and configuring the DIN line as an input. Once this time has elapsed the user can drive the DIN line knowing that a bus conflict will not occur.

[7]The typical time specified for the calibration times is for a master clock of 6 MHz.

Specifications subject to change without notice.

TYPICAL TIMING DIAGRAMS

Figures 2 and 3 show typical read and write timing diagrams for serial Interface Mode 2. The reading and writing occurs after conversion in Figure 2, and during conversion in Figure 3. To attain the maximum sample rate of 285 kHz, reading and writing must be performed during conversion as in Figure 3. At least 330 ns acquisition time must be allowed (the time from the falling edge of BUSY to the next rising edge of $\overline{\text{CONVST}}$) before the next conversion begins to ensure that the part is settled to the 14-bit level. If the user does not want to provide the $\overline{\text{CONVST}}$ signal, the conversion can be initiated in software by writing to the control register.

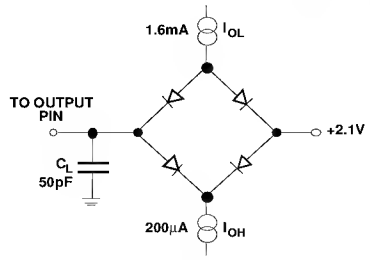


Figure 1. Load Circuit for Digital Output Timing Specifications

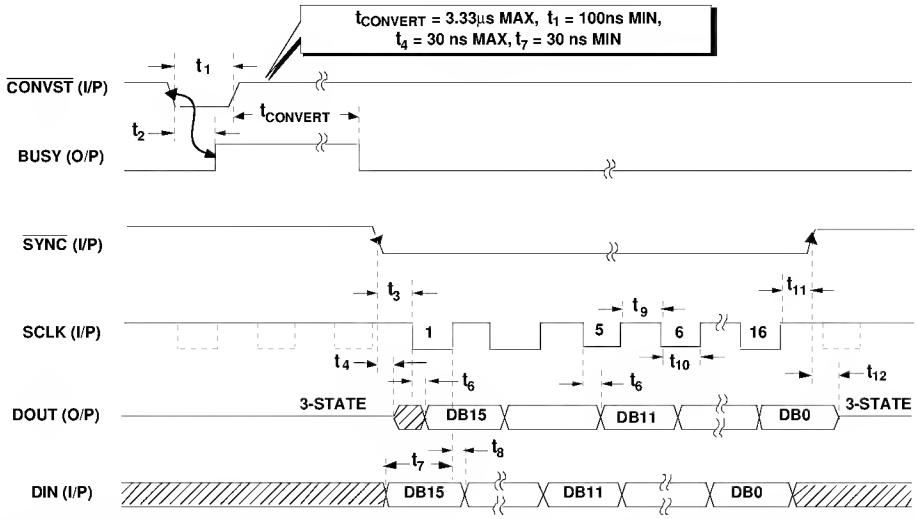


Figure 2. AD7856 Timing Diagram for Interface Mode 2 (Reading/Writing After Conversion)

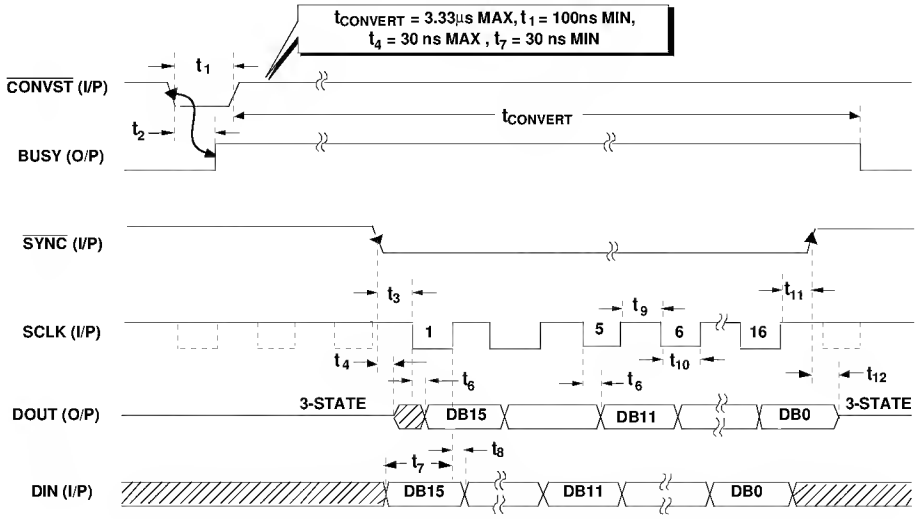


Figure 3. AD7856 Timing Diagram for Interface Mode 2 (Reading/Writing During Conversion)

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

AV_{DD} to AGND ..... –0.3 V to +7 V
DV_{DD} to DGND ..... –0.3 V to +7 V
AV_{DD} to DV_{DD} ..... –0.3 V to +0.3 V
Analog Input Voltage to AGND .... –0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND .... –0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND ... –0.3 V to DV_{DD} + 0.3 V
REF_{IN}/REF_{OUT} to AGND ..... –0.3 V to AV_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[2] .....±10 mA
Operating Temperature Range
  Commercial (A, B Versions) .....–40°C to +85°C
  Storage Temperature Range .....–65°C to +150°C
Junction Temperature ..... +150°C
Plastic DIP Package, Power Dissipation .....450 mW
  θ_{JA} Thermal Impedance ..... 105°C/W
  θ_{JC} Thermal Impedance ..... 34.7°C/W
  Lead Temperature, (Soldering, 10 secs) ..... +260°C
SOIC, SSOP Package, Power Dissipation .....450 mW
  θ_{JA} Thermal Impedance ... 75°C/W (SOIC) 115°C/W (SSOP)
  θ_{JC} Thermal Impedance ....25°C/W (SOIC) 35°C/W (SSOP)
  Lead Temperature, Soldering
    Vapor Phase (60 secs) ..... +215°C
    Infared (15 secs) ..... +220°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch up.

CAUTION

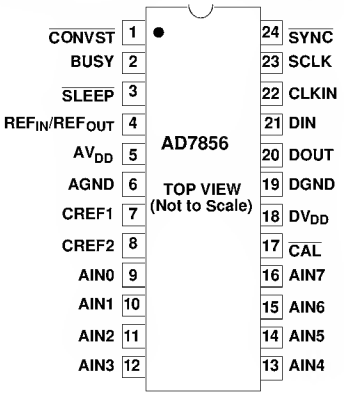
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Linearity Error (LSB)[1]	Package Option[2]
AD7856AN	±2	N-24
AD7856KN	±1	N-24
AD7856AR	±2	R-24
AD7856KR	±1	R-24
AD7856ARS[3]	±2	RS-24
EVAL-AD7856CB[4]		
EVAL-CONTROL BOARD[5]		

NOTES
[1]Linearity error here refers to integral linearity error.
[2]N = Plastic DIP; R = SOIC; RS = SSOP.
[3]L signifies the low power version.
[4]This can be used as a stand-alone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.
[5]This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

PINOUTS FOR DIP, SOIC AND SSOP



TERMINOLOGY[1]

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Total Unadjusted Error
This is the deviation of the actual code from the ideal code taking all errors into account (Gain, Offset, Integral Nonlinearity, and other errors) at any point along the transfer function.

Unipolar Offset Error
This is the deviation of the first code transition (00 . . . 000 to 00 . . . 001) from the ideal AIN(+) voltage (AIN(–) + 1/2 LSB).

Positive Full-Scale Error
This is the deviation of the last code transition from the ideal AIN(+) voltage (AIN(–) + Full Scale – 1.5 LSB) after the offset error has been adjusted out.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of crosstalk between the channels. It is measured by applying a full-scale 25 kHz signal to the other seven channels and determining how much that signal is attenuated in the channel of interest. The figure given is the worst case for all channels.

Track/Hold Acquisition Time
The track/hold amplifier returns into track mode and the end of conversion. Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\text{Signal to (Noise + Distortion)} = (6.02\ N + 1.76)\ \text{dB}$$

Thus for a 12-bit converter, this is 74 dB.

[1]AIN(+) refers to the positive input of the pseudo differential pair, and AIN(–) refers to the negative analog input of the pseudo differential pair or to AGND depending on the channel configuration.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7858/AD7858L, it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2)}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m or n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

Testing is performed using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves, while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

Power Supply Rejection Ratio

Power Supply Rejection Ratio (PSRR) is defined as the ratio of the power in ADC output at frequency f to the power of the full-scale sine wave applied to the supply supply voltage (Vdd). The units are in LSB, %of FS per % of supply voltage, or expressed logrithmically, in dB (PSRR (dB) = 10 log(Pf/Pfs)).

Full Power Bandwidth

The Full Power Bandwidth(FPBW) of the AD7856 is that frequency at which the amplitude of the reconstructed (using FFTs) fundamental (neglecting harmonics and SNR) is reduced by 3dB for a full scale input.

AD7856 PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	$\overline{\text{CONVST}}$	Convert Start. Logic Input. A low to high transition on this input puts the track/hold into its hold mode and starts conversion. When this input is not used, it should be tied to DV_{DD}.
2	BUSY	Busy Output. The busy output is triggered high by the falling edge of $\overline{\text{CONVST}}$ or rising edge of $\overline{\text{CAL}}$, and remains high until conversion is completed. BUSY is also used to indicate when the AD7856 has completed its on-chip calibration sequence.
3	$\overline{\text{SLEEP}}$	Sleep Input/Low Power Mode. A Logic 0 initiates a sleep, and all circuitry is powered down including the internal voltage reference provided there is no conversion or calibration being performed. Calibration data is retained. A Logic 1 results in normal operation. See Power-Down section for more details.
4	REF_{IN}/REF_{OUT}	Reference Input/Output. This pin is connected to the internal reference through a series resistor and is the reference source for the analog-to-digital converter. The nominal reference voltage is 4.096 V and this appears at the pin. This pin can be overdriven by an external reference or can be taken as high as AV_{DD}. When this pin is tied to AV_{DD}, the C_{REF1} pin should also be tied to AV_{DD}.
5	AV_{DD}	Analog Positive Supply Voltage, +5.0 V ±5%.
6	AGND	Analog Ground. Ground reference for track/hold, reference and DAC.
7	C_{REF1}	Reference Capacitor (0.1 μF Multilayer Ceramic). This external capacitor is used as a charge source for the internal DAC. The capacitor should be tied between the pin and AGND.
8	C_{REF2}	Reference Capacitor (0.01 μF Ceramic Disc). This external capacitor is used in conjunction with the on-chip reference. The capacitor should be tied between the pin and AGND.
9–16	AIN1–AIN8	Analog Inputs. Eight analog inputs that can be used as eight single ended inputs (referenced to AGND) or four pseudo differential inputs. Channel configuration is selected by writing to the control register. Both the positive and negative inputs cannot go below AGND or above AV_{DD} at any time. Also the positive input cannot go below the negative input. See Table III for channel selection.
17	$\overline{\text{CAL}}$	Calibration Input. This pin has an internal pull-up current source of 0.15 μA. A Logic 0 on this pin resets all logic and initiates a calibration on its rising edge. There is the option of connecting a 100 nF capacitor from this pin to AGND to allow for an automatic self-calibration on power-up. This input overrides all other internal operations.
18	DV_{DD}	Digital Supply Voltage, +5.0 V ±5%..
19	DGND	Digital Ground. Ground reference point for digital circuitry.
20	DOUT	Serial Data Output. The data output is supplied to this pin as a 16-bit serial word.
21	DIN	Serial Data Input. The data to be written is applied to this pin in serial form (16-bit word). This pin can act as an input pin or as a I/O pin depending on the serial interface mode the part is in (see Table XI).
22	CLKIN	Master clock signal for the device (6 MHz). Sets the conversion and calibration times.
23	SCLK	Serial Port Clock. Logic Input. The user must provide a serial clock on this input.
24	$\overline{\text{SYNC}}$	Frame Sync. Logic Input. This pin is level triggered active low and frames the serial clock for the read and write operations (see Table XI).

AD7856 ON-CHIP REGISTERS

The AD7856 powers up with a set of default conditions. The only writing that is required is to select the channel configuration. Without performing any other write operations the AD7856 still retains the flexibility for performing a full power-down, and a full self-calibration.

Extra features and flexibility such as performing different power-down options, different types of calibrations including system calibration, and software conversion start can be selected by further writing to the part.

The AD7856 contains a **Control Register**, **ADC Output Data Register**, **Status Register**, **Test Register** and **10 Calibration Registers**. The control register is write only, the ADC output data register and the status register are read only, and the test and calibration registers are both read/write registers. The Test Register is used for testing the part and should not be written to.

Addressing the On-Chip Registers

Writing

A write operation to the AD7856 consists of 16 bits. The two MSBs, ADDR0 and ADDR1, are decoded to determine which register is addressed, and the subsequent 14 bits of data are written to the addressed register. It is not until all 16 bits are written that the data is latched into the addressed registers. Table I shows the decoding of the address bits while Figure 4 shows the overall write register hierarchy.

Table I. Write Register Addressing

ADDR1	ADDR0	Comment
0	0	This combination does not address any register so the subsequent 14 data bits are ignored.
0	1	This combination addresses the **TEST REGISTER**. The subsequent 14 data bits are written to the test register.
1	0	This combination addresses the **CALIBRATION REGISTERS**. The subsequent 14 data bits are written to the selected calibration register.
1	1	This combination addresses the **CONTROL REGISTER**. The subsequent 14 data bits are written to the control register.

Reading

To read from the various registers the user must first write to Bits 6 and 7 in the Control Register, RDSLT0 and RDSLT1. These bits are decoded to determine which register is addressed during a read operation. Table II shows the decoding of the read address bits while Figure 5 shows the overall read register hierarchy. The power-up status of these bits is 00 so that the default read will be from the ADC output data register.

Once the read selection bits are set in the Control Register, all subsequent read operations that follow will be from the selected register until the read selection bits are changed in the Control Register.

Table II. Read Register Addressing

RDSLT1	RDSLT0	Comment
0	0	All successive read operations will be from **ADC OUTPUT DATA REGISTER**. This is the power up default setting. There will always be 4 leading zeros when reading from the ADC Output Data Register.
0	1	All successive read operations will be from **TEST REGISTER**.
1	0	All successive read operations will be from **CALIBRATION REGISTERS.**
1	1	All successive read operations will be from **STATUS REGISTER**.

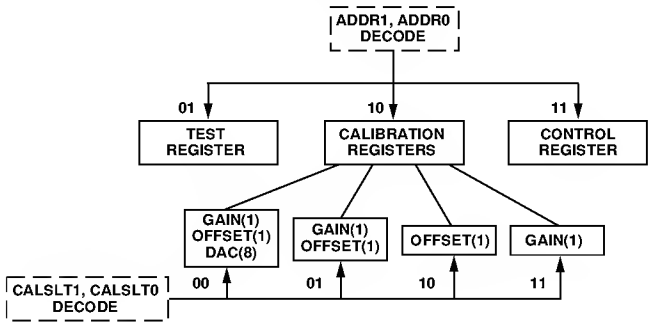


Figure 4. Write Register Hierarchy/Address Decoding

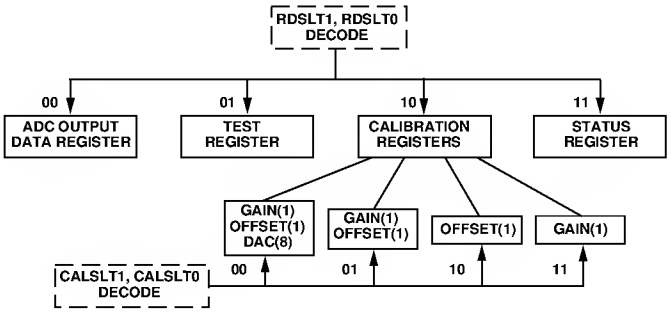


Figure 5. Read Register Hierarchy/Address Decoding

CONTROL REGISTER

The arrangement of the Control Register is shown below. The control register is a write only register and contains 14 bits of data. The control register is selected by putting two 1s in ADDR1 and ADDR0. The function of the bits in the control register are described below. The power-up status of all bits is 0.

MSB

SGL/$\overline{\text{DIFF}}$	CH2	CH1	CH0	PMGT1	PMGT0	RDSLT1

RDSLT0	2/$\overline{3}$ MODE	CONVST	CALMD	CALSLT1	CALSLT0	STCAL

LSB

CONTROL REGISTER BIT FUNCTION DESCRIPTION

Bit	Mnemonic	Comment
13	SGL/$\overline{\text{DIFF}}$	A 0 in bit position configures the input channels in pseudo differential mode. A 1 in this bit position configures the input channels in single ended mode (see Table III).
12 11 10	CH2 CH1 CH0	These three bits are used to select the channel on which the conversion is performed. The channels can be configured as eight single ended channels or four pseudo differential channels. The default selection is AIN1 for the positive input and AIN2 for the negative input (see Table III for channel selection).
9 8	PMGT1 PMGT0	Power Management Bits. These two bits are used with the $\overline{\text{SLEEP}}$ pin for putting the part into various Power-Down Modes (see Power-Down section for more details).
7 6	RDSLT1 RDSLT0	Theses two bits determine which register is addressed for the read operations (see Table II).
5	2/$\overline{3}$ MODE	Interface Mode Select Bit. With this bit set to 0, Interface Mode 2 is enabled. With this bit set to 1, Interface Mode 1 is enabled where DIN is used as an output as well as an input. This bit is set to 0 by default after every read cycle; thus when using the Two-Wire Interface Mode, this bit needs to be set to 1 in every write cycle.
4	CONVST	Conversion Start Bit. A logic one in this bit position starts a single conversion, and this bit is automatically reset to 0 at the end of conversion. This bit may also used in conjunction with system calibration (see Calibration section.)
3	CALMD	Calibration Mode Bit. A 0 here selects self calibration, and a 1 selects a system calibration (see Table IV).
2 1 0	CALSLT1 CALSLT0 STCAL	Calibration Selection Bits and Start Calibration Bit. These bits have two functions. With the STCAL bit set to 1 the CALSLT1 and CALSLT0 bits determine the type of calibration per formed by the part (see Table IV). The STCAL bit is automatically reset to 0 at the end of calibration. With the STCAL bit set to 0 the CALSLT1 and CALSLT0 bits are decoded to address the calibration register for read/write of calibration coefficients (see section on the Calibration Registers for more details).

Table III. Channel Selection

SGL/$\overline{\text{DIFF}}$	CH2	CH1	CH0	AIN(+)*	AIN(–)*
0	0	0	0	AIN_1	AIN_2
0	0	0	1	AIN_3	AIN_4
0	0	1	0	AIN_5	AIN_6
0	0	1	1	AIN_7	AIN_8
0	1	0	0	AIN_2	AIN_1
0	1	0	1	AIN_4	AIN_3
0	1	1	0	AIN_6	AIN_5
0	1	1	1	AIN_8	AIN_7
1	0	0	0	AIN_1	AGND
1	0	0	1	AIN_3	AGND
1	0	1	0	AIN_5	AGND
1	0	1	1	AIN_7	AGND
1	1	0	0	AIN_2	AGND
1	1	0	1	AIN_4	AGND
1	1	1	0	AIN_6	AGND
1	1	1	1	AIN_8	AGND

*AIN(+) refers to the positive input seen by the AD7856 sample and hold circuit,
AIN(–) refers to the negative input seen by the AD7856 sample and hold circuit.

Table IV. Calibration Selection

CALMD	CALSLT1	CALSLT0	Calibration Type
0	0	0	A **Full Internal Calibration** is initiated where the Internal DAC is calibrated followed by the Internal Gain Error, and finally the Internal Offset Error is calibrated out. This is the default setting.
0	0	1	Here the **Internal Gain Error** is calibrated out followed by the **Internal Offset Error** is calibrated out.
0	1	0	This calibrates out the **Internal Offset Error** only.
0	1	1	This calibrates out the **Internal Gain Error** only.
1	0	0	A **Full System Calibration** is initiated here where first the Internal DAC is calibrated followed by the System Gain Error, and finally the System Offset Error is calibrated out.
1	0	1	Here the **System Gain Error** is calibrated out followed by the **System Offset Error**.
1	1	0	This calibrates out the **System Offset Error** only.
1	1	1	This calibrates out the **System Gain Error** only.

STATUS REGISTER

The arrangement of the Status Register is shown below. The status register is a read only register and contains 16 bits of data. The status register is selected by first writing to the control register and putting two 1s in RDSLT1 and RDSLT0. The function of the bits in the status register are described below. The power-up status of all bits is 0.

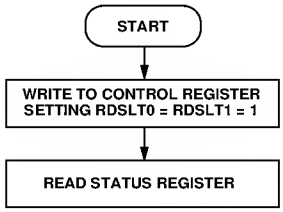


Figure 6. Flow Chart for Reading the Status Register

MSB

ZERO	BUSY	SGL/$\overline{\text{DIFF}}$	CH2	CH1	CH0	PMGT1	PMGT0
RDSLT1	RDSLT0	2/$\overline{3}$ MODE	X	CALMD	CALSLT1	CALSLT0	STCAL

LSB

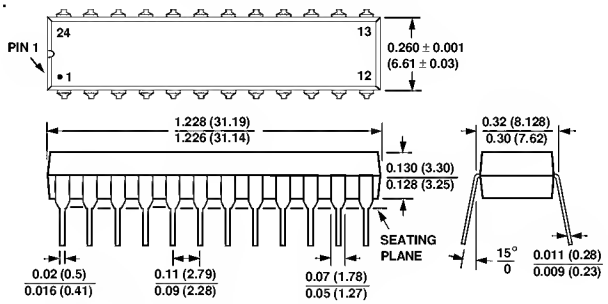
STATUS REGISTER BIT FUNCTION DESCRIPTION

Bit	Mnemonic	Comment
15	ZERO	This bit is always 0.
14	BUSY	Conversion/Calibration Busy Bit. When this bit is 1 this indicates that there is a conversion or calibration in progress. When this bit is 0, there is no conversion or calibration in progress.
13 12 11 10	SGL/$\overline{\text{DIFF}}$ CH2 CH1 CH0	These four bits indicates the channel which is selected for conversion (see Table III).
9 8	PMGT1 PMGT0	Power management bits. These bits along with the $\overline{\text{SLEEP}}$ pin will indicate if the part is in a power down mode or not. See Table VI for description.
7 6	ONE ONE	Both theses bits are always 1 indicating it is the status register which is being read (see Table II).
5	2/$\overline{3}$ MODE	Interface Mode Select Bit. With this bit 0, the device is in Interface Mode 2. With this bit 1, the device is in Interface Mode 1. This bit is reset to 0 after every read cycle.
4	X	Don't care bit.
3	CALMD	Calibration Mode Bit. A 0 in this bit indicates a self calibration is selected, and a 1 in this bit indicates a system calibration is selected (see Table III).
2 1 0	CALSLT1 CALSLT0 STCAL	Calibration Selection Bits and Start Calibration Bit. The STCAL bit is read as a 1 if a calibration is in progress and as a 0 if there is no calibration in progress. The CALSLT1 and CALSLT0 bits indicate which of the calibration registers are addressed for reading and writing (see section on the Calibration Registers for more details).

OUTLINE DIMENSIONS

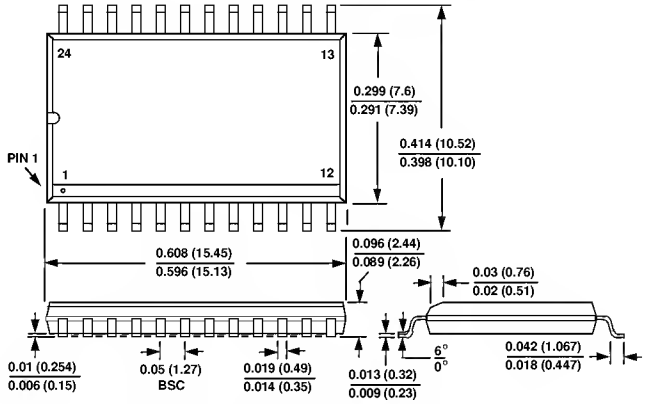
Dimensions shown in inches and (mm).

24-Lead Plastic DIP (N-24)



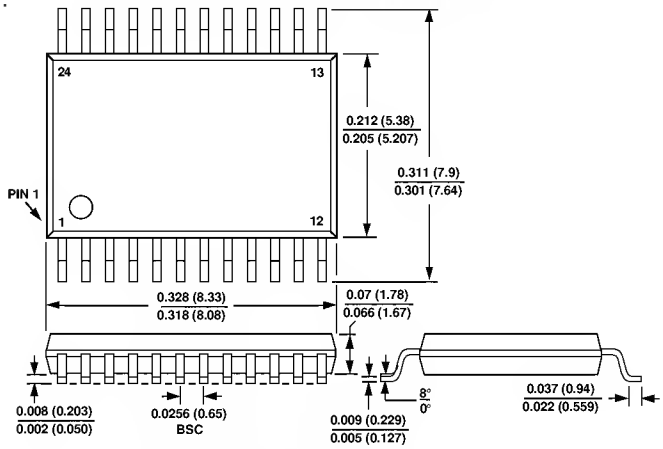
NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
2. PLASTIC LEADS WILL BE EITHER SOLDER DIPPED OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

24-Lead Small Outline Package (R-24)



1. LEAD NO. 1 IDENTIFIED BY A DOT.
2. SOIC LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS

24-Lead Shrink Small Outline Package (RS-24)



1. LEAD NO. 1 IDENTIFIED BY A DOT.
2. LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS